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Supplemental Information Disclosure Statement (4 pages); Form PTO/SB/08A (3 pages) with copies of listed documents (17 documents).

Invention:	SOLDER MASKS FOR USE ON CARRIER SUBSTRATES, CARRIER SUBSTRATES AND SEMICONDUCTOR DEVICE ASSEMBLIES INCLUDING SUCH SOLDER MASKS, AND METHODS
Applicant(s):	Tan et al.
Filing Date:	August 18, 2003
Serial No.:	10/642,908
Date Sent:	January 7, 2004 via first class mail
Docket No.:	2269-5163.1US
TLW/sls:rmh	

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Tan et al.

Serial No.: 10/642,908

Filed: August 18, 2003

For: SOLDER MASKS FOR USE ON CARRIER SUBSTRATES, CARRIER SUBSTRATES AND SEMICONDUCTOR DEVICE ASSEMBLIES INCLUDING SUCH SOLDER MASKS, AND METHODS

Examiner: Unknown

Group Art Unit: 3712

Attorney Docket No.: 2269-5163.1US
(01-0910.00/US)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

January 7, 2004
Date

Rachael M. Harris
Signature

Rachael M. Harris
Name (Type/Print)

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 or PTO/SB/08 be considered by the Examiner and made of record. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

U.S. Patent No.	Publication Date	Patentee
6,251,488	06/26/01	Miller et al.
6,259,962	07/10/01	Gothait
6,268,584	07/31/01	Keicher et al.
6,391,251	05/21/02	Keicher et al.

Other Documents

U.S. Patent Application Publication 2002/0171177 A1 to Kritchman et al., dated November 21, 2002

U.S. Patent Application Publication 2003/0043360 A1 to Farnworth, dated March 6, 2003

U.S. Patent Application Publication 2003/0151167 A1 to Kritchman et al., dated August 14, 2003

U.S. Patent Application Publication 2003/0207213 A1 to Farnworth, dated November 6, 2003

MILLER et al., "Maskless Mesoscale Materials Deposition", Deposition Technology, September 2001, pages 20-22

MILLER, "New Laser-Directed Deposition Technology", Microelectronic Fabrication, August 2001, page 16

Webpage, Objet Prototyping the Future, "Objet FullCure700 Series", 1 page

Webpage, Objet Prototyping the Future, "How it Works", 2 pages

U.S. Patent Application No. 10/191,424, filed July 8, 2002, entitled "Semiconductor Devices With Permanent Polymer Stencil and Method for Manufacturing the Same", inventor Farnworth et al.

U.S. Patent Application No. 10/201,208, filed July 22, 2002, entitled "Thick Solder Mask for Confining Encapsulant Material Over Selected Locations of a Substrate, Assemblies Including the Solder Mask, and Methods," inventor Grigg et al.

U.S. Patent Application No. 10/370,755, filed February 20, 2003, entitled "Chip Scale Package Structures and Method of Forming Conductive Bumps Thereon", inventor Warren M. Farnworth

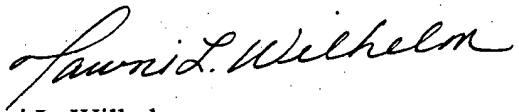
U.S. Patent Application No. 10/672,098, filed September 26, 2003, entitled "Apparatus and Methods for Use in Stereolithographic Processing of Components and Assemblies", inventor Warren M. Farnworth

U.S. Patent Application No. 10/688,354, filed October 17, 2003, entitled "Thick Solder Mask for Confining Encapsulant Material Over Selected Locations of a Substrate and Assemblies Including the Solder Mask", inventor Grigg et al.

Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits.

Respectfully submitted,



Tawni L. Wilhelm
Registration No. 47,456
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: January 7, 2004
TLW/sls:rmh

Enclosures: Form PTO-1449 or PTO/SB/08
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 2 of 3

Complete if Known	
Application Number	10/642,908
Filing Date	August 18, 2003
First Named Inventor	Tan et al.
Group Art Unit	3712
Examiner Name	Unknown
Attorney Docket Number	5163.1US (01-0910.01/US)

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		U.S. Patent Application Publication 2002/0171177 A1 to Kritchman et al., dated November 21, 2002	
		U.S. Patent Application Publication 2003/0043360 A1 to Farnworth, dated March 6, 2003	
		U.S. Patent Application Publication 2003/0151167 A1 to Kritchman et al., dated August 14, 2003	
		U.S. Patent Application Publication 2003/0207213 A1 to Farnworth, dated November 6, 2003	
		MILLER et al., "Maskless Mesoscale Materials Deposition", Deposition Technology, September 2001, pages 20-22	
		MILLER, "New Laser-Directed Deposition Technology", Microelectronic Fabrication, August 2001, page 16	
		Webpage, Objet Prototyping the Future, "Objet FullCure700 Series", 1 page	
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		U.S. Patent Application No. 10/191,424, filed July 8, 2002, entitled "Semiconductor Devices With Permanent Polymer Stencil and Method for Manufacturing the Same", inventor Farnworth et al.	
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Examiner Signature		Date Considered	

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[1] Unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.